AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (currently amended) [[A]] An LSI semiconductor device comprising:

a plurality of processing elements; and

a single switcher that connects each of the plural processing elements to each other,

wherein each of the plural processing elements includes a network interface and is connected to the single switcher via the network interface,

wherein the plural processing elements are located ~~around~~ at a plurality of sides of the single switcher, [[and]]

wherein one of the plural processing elements and the single switcher are connected by peer-to-peer connection via at least one transmission line, and

wherein a connection path between said plural processors forms a system LSI.

2. (canceled)

3. (previously presented) The semiconductor device of claim 1, wherein the switcher is located at the center position of the semiconductor device.

4. (currently amended) The semiconductor device of claim 1, wherein the plural processing elements and the single switcher are implemented in a single semiconductor chip to form a chip LSI.

5. (previously presented) The semiconductor device of claim 1, wherein the plural processing elements and the single switcher are implemented in a single package.

6. (canceled)

7. (previously presented) The semiconductor device of claim 1, wherein each of the plural processing elements has a function of the same hierarchical level.

8. (previously presented) The semiconductor device of claim 1, wherein at least one of the plural processing elements and the single switcher are located in a space where light is confined, and each of the at least one of the plural processing elements and the single switcher has a light emitting element and a light receiving element, wherein an optical communication is performed between the at least one of the plural processing elements and the single switcher.

9. (currently amended) The semiconductor device of claim [[1]] 4 further comprising:

a plurality of semiconductor chips each of which includes plural processing elements and a single switcher; and

at least one inter-switcher which connects the semiconductor chips to each other.

10. (canceled)

11. (previously presented) The semiconductor device of claim 9, wherein the inter-switcher is located in one of the plural semiconductor chips, and the plural semiconductor chips are implemented on a plurality of stacked packages.

12. (currently amended) The semiconductor device of claim 9, wherein each ~~of the~~ switcher of the plural semiconductor chips and the inter-switcher is structured and arranged to have a circuit switching function.

13. (previously presented) The semiconductor device of claim 1, wherein each of the plural processing elements are only connected to the single switcher, through each respective network interface.

14. (currently amended) [[A]] An LSI semiconductor device comprising:

a plurality of LSI peripheral input/output processing elements;

a core processor; and

a single LSI switcher that connects each of the plural peripheral processing elements and the core processor to each other,

wherein each of the plural peripheral processing elements and the core processor includes a network interface and are connected to the single switcher via a respective network interface,

wherein the plural processing elements are located around the single switcher, and

wherein one of the plural processing elements and the single switcher are connected by peer-to-peer connection via at least one transmission line.

15. (new) An LSI semiconductor device comprising:

a plurality of peripheral input/output processing dies;

a core processor die; and

a single switcher die that connects each of the plural processing dies and the core processor die to each other,

wherein each of the plural processing dies and the core processor die includes a network interface and are connected to the single switcher die via a respective network interface, and

wherein the plural peripheral input/output processing dies are located around the single switcher die to form a system LSI.

16. (new) The semiconductor device of claim 8, wherein the light is confined by a sealing resin.

17. (new) An LSI semiconductor device comprising:

a plurality of stacked packages connected via a communication path to form a system LSI,

wherein at least one of the plural packages comprises a plurality of processing modules and a switcher, each of said plural processing modules comprising a network interface connected to said switcher so that the respective plural processing modules can communicate with one another through said switcher.

18. (new) The semiconductor device as claimed in claim 17, further comprising an inter-switcher on one of said plural packages which connects said plural packages to each other.